The Anatomy of the ARM Cortex-M0+ Processor

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What is the Cortex-M0+ Processor?

- **2009** – ARM® Cortex™-M0 processor released
  - Low gate count
  - High performance
  - Easy to use
  - Debug features

- **2012** – Cortex-M0+ processor released
  - Same instruction set
  - Supports all existing features of Cortex-M0
  - New features
  - Higher energy efficiency
  - Ready for future applications
What’s new?

- Even better power efficiency
  - Clean sheet design – 2 stage pipeline
  - Better performance at the same frequency
- Unprivileged execution level
- 8 region Memory Protection Unit (MPU)
- Faster I/O accesses
- Vector table relocation
- Low cost trace solution available
- Various silicon integration features
  (e.g. 16-bit flash support)
Why a New Design?

Energy is the Key

- Embedded products need even longer battery life
  - Need to have lower active power
  - But not compromise on performance

- Low power control applications
  - Need to have faster I/O capability
  - But not higher operating frequency

- Smarter designs
  - Need more sophisticated features
  - But not bigger silicon
Overview of the Cortex-M0+ Processor

- Processor
  - ARMv6-M architecture
  - Easy to use, C friendly
  - Cortex-M series compatibility

- Nested Vectored Interrupt Controller (NVIC)
  - Flexible interrupt handling
  - WIC support

- Memory Protection Unit (MPU)

- Debug from just 2 pins
Compact Instruction Set

- Only 56 Instructions
  - 100% compatible with existing Cortex-M0 processor

- Mostly 16-bit instructions

- All instructions operate on the 32-bit registers

- Option for single cycle 32x32 multiply

Upward compatibility to the ARM Cortex-M3/Cortex-M4
Interrupt Handling

- Nested Vectored Interrupt Controller (NVIC)
  - Interrupt prioritization
  - Interrupt masking
  - Nested interrupt handling

- Ease of use
  - Interrupt handlers in C
  - Processor hardware handles stacking
  - No hidden software overhead
  - CMSIS-Core functions for NVIC control

Cortex-M0+

- NVIC
- Core
- Up to 32 IRQs
- NMI
- SysTick
- System exceptions

ARMv6-M

- Priority level register
- 7 6 0
- Higher priority
- -2
- -1
- 0x00
- 0x40
- 0x80
- 0xC0
- NMI
- HardFault
- IRQs
Low Power Processor Design

- Minimizing power at every opportunity
  - Small silicon area (from 12K gates)
  - Various low power techniques (clock gating, power gating, SRPG, etc)

- 2-stage pipeline processor for maximum energy efficiency
  - Reduce ratio between flip-flops and combinatorial logic
  - Lower average CPI (Cycles Per Instruction)
Sleep Modes

- Architecture defined sleep modes
  - Normal sleep
  - Deep sleep
  - Deep sleep with SRPG support (using WIC) – nW power profile with instant wakeup (processor power down with state retention)
- Can be extended with MCU specific power control registers

Power consumption diagram:

- Power Off
- State Retention only
- Leakage only
- Leakage + some dynamic
- Deep Sleep (WIC)
- Sleep
- Active

Leakage + dynamic

Not to scale
Low Power Features

- **Wakeup Interrupt Controller (WIC)**
  - Detect interrupt while the processor is powered down
  - Enables SRPG deep sleep operation with instant wakeup

- **Sleep-on-exit**
  - Enables the processor to sleep automatically when all interrupt services are complete
  - Ideal for interrupt driven application
Minimizing Flash Accesses

- Program memory access (e.g. Flash) generally on alternate cycles
  - Typical execution of contiguous code shown here
  - A 32-bit fetch gives two 16-bit instructions
Smaller Branch Shadow

- In pipelined processors, subsequent instructions are fetched while executing current instructions (“prefetching”)

- Branch shadow means energy wasted if branch is taken
- Length of branch shadow depends on the alignment of branch instructions

- By moving to a two stage pipeline, the branch shadow is reduced

Maximum branch shadow is 2 instructions (1 word) and minimum is 0 instruction
Cortex-M0+: The Ultimate in Low Power

- The most energy efficient 32-bit processor ever designed
  - Bringing down processor consumption as low as 9µA/MHz*
  - Up to 30% lower power than Cortex-M0

*TSMC 90LP, 1.2V, min. configuration

<table>
<thead>
<tr>
<th></th>
<th>180ULL (7-track, typical 1.8v, 25C)</th>
<th>90LP (7-track, typical 1.2v, 25C)</th>
<th>40G (9-track, typical 0.9v, 25C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum Config*</td>
<td>0.13mm²</td>
<td>0.04mm²</td>
<td>0.01mm²</td>
</tr>
<tr>
<td>Area</td>
<td>52µW/MHz</td>
<td>11µW/MHz</td>
<td>3µW/MHz</td>
</tr>
<tr>
<td></td>
<td>Power (Dhrystone loop)</td>
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<td>Power (Dhrystone loop)</td>
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</tbody>
</table>

- Enabling our partners to develop smaller, smarter and energy friendly solutions for:
  - Pervasive embedded intelligence
  - The upcoming “Internet of Things”
  - Ultimately more electronics and a reduced energy footprint
Small and Powerful

- Benchmarks
  - 1.77 CoreMark/MHz
  - 0.93 DMIPS/MHz
- Lightweight DSP capable

<table>
<thead>
<tr>
<th>Function</th>
<th>Block size</th>
<th>50MHz Runtime</th>
</tr>
</thead>
<tbody>
<tr>
<td>FIR Q15</td>
<td>32 (32 taps)</td>
<td>0.59 ms</td>
</tr>
<tr>
<td>FIR Fast Q15</td>
<td>32 (32 taps)</td>
<td>0.45 ms</td>
</tr>
<tr>
<td>Biquad Cascade Q15</td>
<td>32 (4 stages)</td>
<td>0.30 ms</td>
</tr>
<tr>
<td>Biquad Cascade Fast Q15</td>
<td>32 (4 stages)</td>
<td>0.20 ms</td>
</tr>
<tr>
<td>CFFT Radix4 Q15</td>
<td>64</td>
<td>0.24 ms</td>
</tr>
</tbody>
</table>

- Good fit for entry-level real-time control
High-Code Density

- Smaller flash size needed, leads to:
  - Optimized cost
  - Lower power consumption
  - Smaller chip packages in low pin count devices (sensors, mobile equipments, medical applications, etc)

![CoreMark Code in kB](chart.png)
Single Cycle I/O Interface

- 32-bit simple bus protocol
- Supports 32-/16-/8-bit transfers
- Best suited for accessing
  - GPIO
  - Peripheral registers
- Memory mapped – programmed just like normal peripherals
- Address range(s) defined by silicon designers
- Optional
### Faster I/O Accesses

- **Advantages for applications:**
  - Faster GPIO operations, save precious cycles
  - Better energy efficiency in I/O intensive applications
  - Faster response in FSM replacement applications

- **Example:** Controlling an LCD module with GPIO
  Character output loop – 1 letter/iteration

Clock cycles per loop:
- MSP430 - 12 cycles
- 78K - 10 cycles
- 8051* - 15 cycles
- Cortex-M0+ - 9 cycles

* Optimized assembly code
Memory Protection Unit (MPU)

- Prevents application task from corrupting OS and other tasks’ data
- Improves system reliability
- Up to 8 configurable regions
  - Address
  - Size
  - Memory attributes
  - Access permissions

MPU configuration
Vector Table Relocation

- Vector Table Offset Register (VTOR)
  - Easier system level design (no need to use memory remapping)
  - Flexible vector table configuration

- Relocate vector table to other locations in flash / SRAM
  - Boot loader
  - Exception vector reconfiguration at runtime
Easier Silicon Integration

- Highly configurable
  - Verilog parameters to include features you want e.g.
  - Number of IRQ
  - Debug features
  - I/O interface ...

- New features
  - Start-up delay control (CPUWAIT)
  - 16-bit flash support

- Cortex-M System Design Kit (CMSDK) support available soon
Cortex-M System Design Kit (CMSDK)

- Fast track your design process with CMSDK
  - Easy to use design kit with example system designs
  - Designer can simply plug-in their processor and go!
  - Essential AMBA® interconnects and peripherals
  - Software support - Keil™ examples and CMSIS drivers

Optimised for low area, low power, low latency
Summary – Cortex-M0+

Maximizing energy efficiency
- Clock
- Pre-decode
- Main decode
- Instruction #N
- Fetch
- Decode
- Execute
- Instruction #N+1
- Fetch
- Decode
- Execute

Low-cost, powerful debug and trace
- Microcontroller
  - Debug connector
  - Processor
    - Program execution info
  - AHB interface
  - MTB controller
  - RAM interface
  - SRAM
  - Application Data + Trace Data

Faster I/O accesses
- Data
- Strobe
- “A”
- “B”
- “C”

Maintaining 100% compatibility to enable an immediate ecosystem
- Silicon Partners
- Design Support Partners
- Software-Training and Gumstix Partners

The Architecture for the Digital World®
Thank you