Exploring ARM’s Cache Coherent Network Technology to Handle Exponential Data-Flow Growth

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Information Society Driving Enterprise Data Demands

Mobile/IOT
- From Sensor
- Wireless Networks
- Residential Gateways
- Business Gateways

Network Infrastructure:
- Backbone
- Edge

Network Throughput
- Density
- Scalability
- 1Gb/s to 100Gb/s

Cloud
- To Server
- Advanced RAS
- Choice
- Rapid Innovation
- TCO

Scalable High-Bandwidth I/O
The Architecture for the Digital World®
The Operator Challenges

- **107%**
  LTE Capex CAGR 2010-2014

- **18X**
  Data traffic increase on mobile networks 2011-16

- **~80%**
  Network energy consumption attributable to base stations

Source: Cisco Systems, ISuppli, NSN, IEEE
2013-2016 Infrastructure Trends

- Heterogeneous form factors
- Rapid deployment of new services
- Server capacity at edge
- Scalable processing
- Open software platforms
- 3m small cells forecast (2016)
2013-2016 Enterprise Trends

- IT is the business
- Density, power and cost over raw perf.
- One size no longer fits all
- Optimized highly integrated SoCs
- Open source and end user S/W
- Estimated 20x increase in network traffic
Server/Networking Equipment – Tomorrow…

One size does not fit all → increased server specialization

Software Defined <X>
Accelerated innovation
Flexibility
Manageability
Scalability
Efficiency
Choice

Network flexibility → SDN / NFV

Traditional 2P 2U server

Traditional networking equipment

The Architecture for the Digital World®
ARM Enterprise Building Blocks

Cloud
- Advanced RAS
- Security
- Reliability

Pipe
- Throughput density
- Scalability
- 1Gb-100Gb

Server
- Single-thread Performance
  - Features: 64-bit, ECC
  - Advanced RAS
  - Architecture Licensees
  - Cortex-A15
  - Future
  - Cortex-A7
  - Cortex-A53
  - Cortex-A57

Control Plane
- Scalability
  - CoreLink™ CCN-500 Family
  - Future
  - AMBA® 5 CHI – coherency for scalable efficient performance

Data Plane
- Features
- Acceleration
- Scalability
- Future
- Cortex®-A7
- Cortex-A53
- Future

The Architecture for the Digital World® ARM
LSI Delivers Axxia® 5500 Communication Processor for Faster, More Power-Efficient Networks

World’s first cache-coherent, 16-core SMP ARM processor

……..“With AXM5500 in hand, our customers are developing next-generation networking systems with the performance, intelligence and scalability to keep pace with the unprecedented growth in network traffic,” said Gene Scuteri, vice president of engineering, Networking Solutions Group, LSI. “The Axxia 5500 multicore family, with its unmatched, highly integrated design and broad features, is an ideal platform on which to build high-performance systems.”

Based on CoreLink CCN-504
CoreLink CCN-504 SOC delivered to OEMs
CoreLink CCN-504 suitable for Mobile and fixed networks
Use of CoreLink CCN-504 support a variety of network configurations
Wide deployment of CoreLink CCN-504….. “Represent over half of the mobile base station market”…
CoreLink CCN Pedigree

Physically-Optimized Microarchitecture

- Based on the proven CCN-504 microarchitecture and components:
  - Fully functional silicon running at 1.5 GHz+ in 28 HPM (achieved)
  - Leverages extensive verification: trillions of cycles in simulation, co-emulation with ARM IP
  - Proven, non blocking Architecture (AMBA 5 CHI)/Microarchitecture (CoreLink CCN-504)

Detailed Microarchitectural Performance Model

- Cycle-accurate SystemC performance model: correlated to within 3% of RTL
- Extensive performance tuning with numerous internal and external workloads
- SystemC TLM interfaces for connecting partner IP or ARM-provided traffic generators
CoreLink CCN-508: High-end Networking/Server

- **Virtualized Interrupts**
- Up to 4 cores per cluster
- Up to 8 coherent clusters
- Integrated L3 cache
- Quad channel DDR3/4 x72

**Heterogeneous processors – CPU, GPU, DSP and accelerators**

**ARM CoreLink™ CCN-508 Cache Coherent Network**

- 1-32MB L3 cache
- Snoop Filter
- NIC-400 Network Interconnect
- NIC-400 Network Interconnect
- PCIe
- USB
- SATA
- CPU, GPU, DSP and accelerators
- Virtualized Interrupts
- Uniform System memory
- Peripheral address space
- Up to 24 AMBA interfaces for I/O coherent accelerators and IO

**CoreLink DMC-520**

- Quad Cortex-A57/A53
- L2 cache

**Quad Cortex-A57/A53**

- L2 cache

**Up to 4 cores**

**Up to 8 coherent clusters**

**Integrated L3 cache**

**Quad channel DDR3/4 x72**

**Peripheral address space**

**The Architecture for the Digital World®**
Traffic Mixes in Networking Infrastructure

- CCN Interconnect can scale to different networking solutions which use different traffic mixes
  - You can implement your SOC with ARM CPU, ARM Interconnect and DSP/Accelerators
ARM Networking Use-Cases: BTS

**BTS Application**

- Many-core processing for thread-able workloads
  - CCN-508 based with mix of Cortex-A57 and A53 with acceleration
  - L3 Coherency managed by CCN-508
- BTS, Wireless Backhaul, Radio-Network-Controller
- Security appliances (DPI)
- Clusters of 4 core, moderate frequency

![Diagram of ARM CoreLink™ CCN-508 Cache Coherent Network](image-url)
**ARM Networking Use-Cases: CDN/Core**

**Control Plane/Server Application**

- **EPC, Core Network, Content at Edge.**
- **High-performance, single thread cores**
  - Optimized for high frequency
  - Multiple Cortex-A57/ Next Gen. clusters, low core count per cluster
- **I/O, Storage and Compute Virtualization (KVM/XEN)**

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[Diagram showing CoreLink CCN-508 Cache Coherent Network and control processing.]
ARM Partner designs for the Data Center

- Partners developing variety of solutions
- Leveraging their expertise
- More choices for applications
ARM Partner designs for the Data Center

ARM Processor
- Multi-core
- Quad to 16 core
- 1.4-2.4 GHz
- 32-bit and 64-bit
- ARM Fabric

Calxeda Energy Saver 1000
- EnergyCore Management Engine
- I/O Controllers
- SATA, PCIe, Ethernet, SD/eMMC
- EnergyCore Fabric Switch

Marvell
- System Crossbar
- PCIe
- SATA
- 5 x USB Host/Dev
- 4 x Security Engine

AXE4500 Architecture Diagram
- Network Compute Adapter
- DDR3/4 Controllers
- L3 Cache
- Modular Packet Processor
- Memory Management Engine
- Interfaces & Peripherals
- PPE
- Virtual Pipeline Task Ring

The Architecture for the Digital World®
ARM Partner designs for the Data Center

ARM Processor
Multi-Core
Quad to 16 core
1.4-2.4 GHz
32-bit and 64-bit
ARM Fabric

Partner
differentiated
Fabric, Storage,
Networking
and Security IP
Integration = Increased Density & Reduced TCO
Cortex-A57: Flagship Debut of 64-bit

- Leading the transition to ARMv8
  - Streamlined 64-bit ISA
  - Extended 32-bit functionality
  - Hardware-accelerated cryptography
  - Enhanced IEEE SP/DP floating point
  - Extended soft-error recovery
- Highest Performance for next-generation
  - Improved performance on 32-bit, 64-bit code and floating point
  - Up to 10x improvement on crypto algorithms
  - Larger working sets, better branch prediction
  - Greater focus on memory subsystem
- Extremely scalable system architecture
  - Next-generation CCN for advanced scalable systems

**Cortex-A57 MPCore**

- **Cortex-A57 Core**
  - ARMv8 32b/64b Core
  - NEON SIMD engine
  - Floating Point Unit
  - 48k I-Cache w/Parity
  - 32k D-Cache w/ECC
- **L2 w/ECC (512kB ~ 2MB)**
- **ACP SCU**
- **128-bit AMBA 4 or AMBA 5 CHI Coherent Bus Interface**

**Highest Performance 64-bit ARM Core**
Cortex-A53 – Extreme Power Efficiency

- Power efficient performance
  - In-order, 8-stage, dual-issue pipeline
  - Improved integer, NEON™, FPU, and memory performance
- ARMv8-A
  - 64b support, and 32b w/ AArch32
  - Architectural enhancements
- Scalable for many markets
  - big.LITTLE™ companion to Cortex-A57
  - AMBA4 ACE and AMBA 5 CHI interfaces

The Most Efficient 64b Core

The Architecture for the Digital World®
High Performance Memory Access

CoreLink DMC-520

- 5th Generation ARM DMC
  - ECC and RAS features
  - Performance Profiling
  - TrustZone Address Space Control

- End to end traffic management
  - System wide QoS, designed and verified with ARM CPUs and CoreLink CCN

Performance
- Max bandwidth > 21GB/s per channel
  - Buffering to optimize read/write turnaround

Interfaces
- AMBA 5 CHI direct connection to CCN-508
  - Industry standard DFI-3.0 to connect to PHY

Memory
- Support for x72 DRAM
  - DDR3, DDR3L and DDR4 up to DDR4-2667

Low Power Support
- Programmable DRAM power modes
CoreLink End-to-End QoS Architecture

Enterprise Requirements
- “Bursty” Datapath
  - High peak bandwidth
  - Multiple interfaces
- “Compute intensive” Control Path
  - Lowest latency requirements
- “Latency Sensitive” Air interface
  - Predictable Latency

CoreLink End-to-End QoS
- QoS field for every transaction
  - Fixed, programmable or regulated
  - End-to-End propagation
- Programmable QoS mechanisms
  - Regulation of all traffic on ingress
  - Bandwidth management
  - Latency management
- QoS re-ordering and arbitration
  - Interconnect ingress
  - Non-blocking transport
  - L3 cache
  - DMC
CoreLink CCN-508: Performance

- 250GB/s peak, 160GB/s sustained interconnect bandwidth
- 300GB/s peak IO/accelerator bandwidth (50GB/s per port)*
- Integrated snoop-filter for highly scalable coherency
- Sophisticated end-to-end QoS and system-level power-management
- Quad channel DRAM support for DDR3, DDR3L and DDR4 up to DDR4-2667

* At equivalent processor frequencies
Linaro Networking Group (LNG)

- Vertical subgroup launched Feb’13
- Optimized, open-source *networking platform software for scalable networks*
- Coordinates and multiplies members’ efforts, accelerates product TTM

LNG Members: Sept 2013
Linaro Enterprise Group (LEG)

- Existing and new members will deliver optimized core open-source software for ARM servers

- Reduces costs, eliminates fragmentation, accelerates product time to market

- Enables ARM Server vendors to focus on innovation and differentiated value-add
Summary

Redefining the Server and Network Equipment

CoreLink™ CCN-508 Cache Coherent Network IP

CoreLink™ DMC-520 Dynamic Memory Controller IP

A true partnership = innovation and choice