Building Ultra-Low Power Wearable SoCs
Wearable

noun
An item that can be worn

adjective
Easy to wear, suitable for wearing
Wearable Opportunity: Fastest Growing Market Segment

Projected Growth from 2013 - 2017

- 71%
- 79%
- +400%
- +9%

Source: IDC 2013 (Smartphone, Tablet and Portable PCs, Berg Insight 2013 – Wearables)
ARM® Technology Driving Innovation in the Wearable Market
Wearables - An Extremely Diverse Market

Extremely diverse market that is addressed by the ecosystem around ARM processors

- Professional
- Elderly
- Pets
- Animals
- Teenagers
- Health
- Industrial
- Office
- Lifestyle
- Sports
- Extreme sports
- Kids
Challenges in Wearables Market

Behavioural Challenges
- Personal Connection
- Price
- Social acceptance
- Use cases
- User habits

Technical Challenges
- Fashion drives form factor
- Battery life
- Diverse Requirements
- Evolving Software ecosystem
- Thermal constraints

Use cases still evolving for wearable devices
## Going Hands-free With Wearables

Mobile Users Reach to Phone ~150 Times a Day

<table>
<thead>
<tr>
<th>Activity</th>
<th>Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>Messaging</td>
<td>23</td>
</tr>
<tr>
<td>Voice Call</td>
<td>22</td>
</tr>
<tr>
<td>Checking Time</td>
<td>18</td>
</tr>
<tr>
<td>Other</td>
<td>14</td>
</tr>
<tr>
<td>Music</td>
<td>13</td>
</tr>
<tr>
<td>Gaming</td>
<td>12</td>
</tr>
<tr>
<td>Social Media</td>
<td>9</td>
</tr>
<tr>
<td>Alarm</td>
<td>8</td>
</tr>
<tr>
<td>Camera</td>
<td>8</td>
</tr>
<tr>
<td>News and Alerts</td>
<td>6</td>
</tr>
<tr>
<td>Calendar</td>
<td>5</td>
</tr>
<tr>
<td>Search</td>
<td>3</td>
</tr>
<tr>
<td>Web</td>
<td>3</td>
</tr>
</tbody>
</table>

Source: Tomi Ahonen Almanac 2013
The Battery Life Challenge for Wearables

- **Daily**: 3000 mAH
- **Weekly**: 300 mAH
- **Monthly**: 150 mAH
Key Functionality for Wearable Devices

- High-efficiency Performance, constrained power budget
- Always Aware, Lowest Power
Wearable Systems Architecture

Basic Architecture

Mid Architecture

High-end Architecture

Always On

Apps CPU

Interconnect

FLASH

ROM

SRAM

Always On

Apps CPU

INTERCONNECT

FLASH

ROM

SRAM

DMC

RTOS

Rich OS

Higher Performance

Apps CPU

Always On

GPU

Display Processor

Video Processor

Interconnect

FLASH

ROM

SRAM

DMC

RTOS

Rich OS

Flash

ROM

SRAM

DMC

RTOS

Rich OS

Flash

ROM

SRAM

DMC

RTOS

Rich OS

Flash

ROM

SRAM

DMC

RTOS

Rich OS

Flash

ROM

SRAM

DMC
Always-aware ARM® Cortex®-M CPUs For Wearables

- **Lowest cost**
- **Low power**
- **Outstanding energy efficiency**

- **Performance efficiency**
- **Feature rich connectivity**

Digital Signal Control (DSC) Processor with DSP
- Accelerated SIMD
- Floating point (FP)

ARM® Cortex®-M0+

- CPU
- Nested/Vectored Interrupt Controller
- Memory Protection Unit
- ARM®-Lite Interface
- Data Watchpoint Interface
- SRAM & Peripheral Interface
- Micro Trace Buffer
- Debug Access Port

ARM® Cortex®-M0

- CPU
- Nested/Vectored Interrupt Controller
- Memory Protection Unit
- ARM®-Lite Interface
- Data Watchpoint Interface
- SRAM & Peripheral Interface
- Debug Access Port

ARM® Cortex®-M3

- CPU
- Nested/Vectored Interrupt Controller
- Memory Protection Unit
- ARM®-Lite Interface
- Data Watchpoint Interface
- SRAM & Peripheral Interface
- Debug Access Port

ARM® Cortex®-M4

- CPU (with DSP Extensions)
- Wake Up Interrupt Controller Interface
- Code Interface
- Memory Protection Unit
- SRAM & Peripheral Interface
- Bus Matrix
- Data Watchpoint Interface
- Flash Patch Interface
- Breakpoint Interface
- ITM Trace
- Serial Wire, Trace Port
- Debug Access Port

- DSC Processor with DSP
- Accelerated SIMD
- Floating point (FP)

‘8/16-bit’ Traditional application space

‘16/32-bit’ Traditional application space
High-efficiency ARM® Cortex® A Processors for Wearables

**ARM® Cortex®-A5**
- ARM CoreSight™ Multicore Debug and Trace
- ARMv7 32b CPU
- 4-64k I-Cache
- 4-64k D-Cache
- Core
  - 1
  - 2
  - 3
  - 4
- NEON™ Data Engine
- Floating Point Unit
- ACP
- SCU
- Dual 64-bit AMBA®3 AXI

**ARM® Cortex®-A7**
- ARM CoreSight™ Multicore Debug and Trace
- ARMv7 32b CPU
- 16-64k I-Cache
- 16-64k D-Cache
- Core
  - 1
  - 2
  - 3
  - 4
- NEON™ Data Engine
- Floating Point Unit
- SCU
- L2 Cache
- ACP
- SCU
- 128-bit AMBA® ACE Coherent Bus Interface

**ARM® Cortex®-A53**
- ARM CoreSight™ Multicore Debug and Trace
- ARMv8-A 32b/64b CPU
- B-64k I-Cache w/parity
- B-64k D-Cache w/ECC
- Core
  - 1
  - 2
  - 3
  - 4
- NEON™ SIMD engine with crypto ext.
- ACP
- SCU
- L2 w/ECC (128kB – 2MB)
- Configurable AMBA4 ACE or AMBA5 CHI Coherent Bus Interface

- 8 stage in-order
- Single issue
- **ARMv7-A**
- **AMBA® 3**

- 8 stage in-order
- **ARMv7-A Extensions**
- **AMBA 4 ACE**

- 8 stage in-order
- **Partial dual issue**
- **ARMv7-A Extensions**
- **AMBA 4 ACE**

- 8 stage in-order
- **Full dual issue**
- **ARMv8-A**
- **AMBA 4 or AMBA 5**
Building Lowest-power Wearable SoCs

Right Configuration

Lowest-power Implementation

Right-software Optimization

Mobile

Wearable

Power
ARM® NEON™: Energy-efficient SIMD for Wearable Computing

- Accelerated performance for DSP and media algorithms
- Tightly integrated with CPU pipelines
- Coding and debugging using same tool chain
- Scalable NEON performance across CPUs

Example NEON Use Cases for Wearable Computing

- User Interfaces
- Game processing
- Voice recognition
- Image processing
ARM® NEON™ Ecosystem Advantage for Wearable Solutions

- **Extensive 3rd Party Ecosystem**
  - 2D GUI Library and GUI Visual Effects
  - NEON-optimized Audio and Video Codecs

- **Extensive support in Open Source**
  - **Android** – NEON optimizations
    - Skia library is 5x faster using NEON
  - **Android Wear**: Renderscript MUST be supported by default this is on CPU/NEON

NEON offers several benefits for evolving wearable use cases
Building Lowest-power Wearable SoCs

- Right Configuration
- Lowest-power Implementation
- Right-software Optimization
Optimizing ARM® Cortex®-A CPUs for Wearable Power Envelope

100-150 mW power budget per CPU

Relative to Cortex-A7 MP2, 1.2 GHz

Cortex-A7 MP2 Mobile

SpecInt2k Performance
Total Power

28 nm
Optimizing Cortex-A CPUs for Wearable Power Envelope

100-150 mW power budget per CPU
1.2 - 1.6 GHz

- Cortex-A7 MP2 Mobile: 1.00
- Cortex-A7 MP2 Wearable: 0.38
- Cortex-A5 UP Smallest: 0.10

SpecInt2k Performance
Total Power

- Less than 35 mW per CPU
- 500-800 MHz

All on 28 nm process
Cortex-A7 PPA Optimization for Wearables – 28nm

<table>
<thead>
<tr>
<th>Configuration</th>
<th>Cortex-A7 MP2 (Mobile)</th>
<th>Cortex-A7 MP2 (Wearable)</th>
<th>Cortex-A7 MP1 (Smallest)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Configuration</td>
<td>32K L1, 512K L2, NEON</td>
<td>16K L1, NEON, 128KB L2</td>
<td>8K L1, No NEON, No ETM</td>
</tr>
<tr>
<td>Typical Frequency Target (MHz)</td>
<td>1200 – 1600</td>
<td>400 – 800</td>
<td>400 – 800</td>
</tr>
</tbody>
</table>

Massive reduction in **idle-mode** power consumption

Significant reduction in **active-mode** power consumption
## Ultra-low Power ARM® Cortex®-M CPUs for Always-aware Functions

<table>
<thead>
<tr>
<th></th>
<th>Cortex-M0+</th>
<th>Cortex-M0</th>
<th>Cortex-M3</th>
<th>Cortex-M4</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Freq (MHz)</strong></td>
<td>50</td>
<td>50</td>
<td>50</td>
<td>50</td>
</tr>
<tr>
<td><strong>$P_{\text{dyn}}$ (µW/MHz)</strong></td>
<td>3</td>
<td>4</td>
<td>7</td>
<td>8</td>
</tr>
<tr>
<td><strong>$P_{\text{total}}$ (mW)</strong></td>
<td>0.15</td>
<td>0.2</td>
<td>0.35</td>
<td>0.4</td>
</tr>
<tr>
<td><strong>Area (mm$^2$)</strong></td>
<td>0.009</td>
<td>0.01</td>
<td>0.03</td>
<td>0.04</td>
</tr>
<tr>
<td><strong>CoreMark®/MHz</strong></td>
<td>2.33</td>
<td>2.42</td>
<td>3.32</td>
<td>3.4</td>
</tr>
</tbody>
</table>

**$P_{\text{static}} < 3µW$**

**$P_{\text{total}} < 0.5mW @ 50 MHz$**

All PPA trials at 40G (9-track, typical 0.9v, 25C)
Base usable CPU configuration
CoreMark numbers from [www.coremark.org](http://www.coremark.org)
Building Lowest Power Wearable SoCs

- Right Configuration
- Lowest-power Implementation
- Right-software Optimization
Wearables Optimized for Micro-interactions

High time and interaction cost for “a moment of information”

Reduced overhead per interaction – more present in the real world
Modes of Operation in Android Wear Devices

- **Ambient Mode**
  - Power
  - Sensing
  - Notification
  - Time
  - Date
  - Calendar

- **Interactive Mode**
  - Search
  - Message
  - Audio
  - Video
  - Calling

- **Sleep Mode**
  - Time
Optimizing Modes of Operation in High-end Wearable Devices

<table>
<thead>
<tr>
<th>Device Mode</th>
<th>Operation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Local</td>
<td>Apps run on wearable device</td>
</tr>
<tr>
<td>Head Mounted Display</td>
<td>Apps run on smart phone, display on wearable device</td>
</tr>
<tr>
<td>Collaborative/Interactive</td>
<td>Apps run on both smartphone and wearable device</td>
</tr>
</tbody>
</table>
Summary

- ARM-based solutions are driving innovation in the fast-evolving wearable market

- Wearables require lowest power and always-aware functions, along with high-efficiency on-demand performance

- Right CPU configuration and right ‘sized’ implementation are critical for strict low-power budgets for wearable devices
  - >50% reduction in active power
  - >90% reduction in idle power

- ARM provides complete low-power solutions to meet the performance and lowest power goals for all categories of wearable devices
  - Low power CPU, System IP, GPU and Physical IP for high-end wearable devices