Veloce2® the Enterprise Verification Platform

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Agenda

- Emulation Use Modes
- Veloce® Overview
- ARM® case study
- Conclusion
Emulation Use Modes
Solutions portfolios address all use modes

- In Circuit Emulation
- Simulation Acceleration
- Virtual Lab Emulation
- Software Debug

One Platform – All use modes

- iSolve™ solutions
- VIP /Transactors
- VirtuaLAB and Memories
- JTAG, Virtual Probe, Veloce® Codelink™
Veloce2 Delivers Real Value

- **Design:** Network switch with multiple 10G ports
- **Mode:** Streaming 64-byte packets on all ports

Billions of transactions across all Ethernet ports

Simulation: ~1/4th frame/sec  
Emulation: ~3,662 frames/sec  

~15,000x faster than simulation
Crystal2 Custom Architecture

- Rich interconnect yields 5 minute chip compiles
- Built-in logic analyzer – all signals visible all of the time
- Custom Virtual Wires logic for reliable chip-to-chip routing
- Switched backplane interconnect for board-to-board routing
- Fully automated software to compile designs

Crystal2 → Advanced Logic Board → Veloce2 Quattro

Full custom IC
Maximus: Enterprise Verification Platform

<table>
<thead>
<tr>
<th>Feature</th>
<th>Specification</th>
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<tbody>
<tr>
<td>AVB</td>
<td>Up to 64</td>
</tr>
<tr>
<td>Capacity (user gates)</td>
<td>Up to 1 Billion</td>
</tr>
<tr>
<td>ICE users</td>
<td>Up to 16</td>
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<tr>
<td>TBX or stand alone users</td>
<td>Up to 64</td>
</tr>
<tr>
<td>Physical IOs</td>
<td>Up to 9600 (120*80)</td>
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<tr>
<td>Extended IO</td>
<td>Up to 4X</td>
</tr>
<tr>
<td>Power</td>
<td>50 kW</td>
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<tr>
<td>Noise Level</td>
<td>75 dBA</td>
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Veloce OS3 Enterprise Server

- Consolidates global Veloce resources into a unified high-capacity entity

- Speeds high-priority jobs by suspending jobs of low priority

- Shields emulator complexity from LSF and Netbatch queue managers

- Automatically adapts to change in HW availability
Veloce Enables Full Chip Validation

- The confidence level in the design before tape-out is maximized with full chip emulation
  - System level architectural bugs detection such as Performance, HW-SW tests, Interrupts, Cache configuration, Memory Coherency, interconnect, and others
  - Verifying the integration: interconnect, memory map, clocks, reset sequences
  - Real life HW-SW test cases on OS create sequences that get to corner cases almost impossible to reach in sub-system clusters.
  - Power aware verification.
    - Measuring power metrics is best done with real SW in full chip
    - Verifying different power modes
    - Verifying power with real OS task-switching effects
Full-Chip Validation Prior to Silicon: Boot OS, Drivers Validation

- OS and device drivers run on RTL or ISS processor models
- VirtuaLAB peripherals exercise interfaces
- SW debug solutions
- Power analysis

Codelink Multi-core SW/HW debug
Veloce Peripheral Interface Solutions

Identical IP used for all solution offerings

Peripheral Interface Design IP

Silicon proven

iSolve
Physical Peripherals

VirtuaLAB
Virtual Peripherals

Verification IP
Protocol Transactors

Example Test
Coverag e and Assertio n
Test Plan

Users’ Test Sequences
Accelerated Transactor
Users’ DUT

ARM Tech Symposia 2014
Advantages of VirtuaLAB

- Attractive alternative to ICE
- Ideal for multi-user and multi-project
- VirtuaLAB runs on Linux host
- Peripherals are hardware accurate
- Instantly reconfigured
- Datacenter compatible

Physical Devices to Virtual Devices

Transferring emulation from the lab to datacenter delivers more productivity, flexibility, and reliability
Many Software Engineers at the same time
ARM Case Study
ARM System-level Validation

- Objective is to perform ‘in-system’ validation of ARM IP products, for example:
  - Extended validation of IP products such as CPUs, GPUs and System IP components in a ‘system’ context
    - Aim is to find IP product bugs through real-world testing
    - *(Not the same as a traditional SoC system validation approach)*

- To support this activity, we developed the SystemBench testbench environment as a configurable platform for running system validation tests on emulation and FPGA systems
  - Used for system validation of ARM® Cortex®-A and -R class CPUs, System IP and ARM Mali™ GPUs
  - Current version of SystemBench supporting the ARMv7 and ARMv8 product families
  - SVRIS test generation tools for stress testing
  - Plus many supporting automation flows and infrastructures
Why Emulation?

- **Execution Speed:** ~1 MHz
  - Long running tests, realistic HW/SW scenarios

- **Fast compile and turnaround**
  - Much quicker than FPGA boards

- **Capacity flexibility** – many testbench configurations, many users
  - 12.5 M Gates; up to 400 M Gates on Veloce

- **Debug capability**
  - FSDB dump, Triggers, Vstream

- **VIP and connectivity solution to real-world traffic**
  - Xactor flow, e.g. PCIe, ARM® AMBA® CHI specification, Speedbridge solution

- **Currently able to run ARM® CoreLink™ CCI-400 and ARM CoreLink CCN-504 / 508-based system configuration tools**
  - As large as 200 M Gates, average 60-100 M Gates
SystemBench

- Fully synthesizable and highly configurable
- Automated integration
- Extensible for adding desired synthesizable VIP (traffic gen, irritators)
- Emulation-friendly, build and run automation
SV OS/Apps Testing

- Targeting with combinations of multi-CPU/clusters using ARM CoreLink CCI-400 and ARM CoreLink CCN platforms

- Based on Linux, built for Aarch32 and Aarch64
  - Retargeting existing test suites for Aarch64, where possible

- Stressing with mixed payloads:
  - t32/a32/a64 applications under the same a64 kernel
  - t32/a32/a64 OSes under the same a64 hypervisor
  - t32/a32/a64 secure irritators running EL1/EL0

- Multi-cluster modes; ARM® big.LITTLE™ testing
  - ‘Always on,’ stressing traffic between clusters
  - ‘Switched,’ stressing power down/up
Debug and Visibility

- Debugging any failure at system-level is a significant effort without having the right infrastructure
- Debug traces
- Waveform dump and triggers
- Better control through VIP for reproducibility
- Connectivity to RealView debugger for SW debug
How Veloce Helps the ARM SV Team

- Much larger capacity suitable for enterprise-class system workloads: 100s of M Gates
  - Able to run many more realistic scenarios for networking system configurations

- Near simulation-like visibility, better and faster debug

- Coverage capabilities

- Multiple users on a single emulation box

- Prompt Support from MGC and established communication channels 😊
Going Beyond Simulation Acceleration

Simulation Acceleration
- OVM/UVM
- SystemVerilog
- C/SystemC

Accelerated Transactors

SW Debug
- Codelink
- VProbe
- Warpcore
- QEMU

Software Debug

Virtual Protocol Solutions
- USB
- SATA
- Video
- Ethernet
- PCIe

VirtuaLAB Solutions

Physical Protocol Solutions
- PCIe
- SATA
- Video
- USB
- Ethernet

iSolve Solutions

Co-Model Channels

Testbench Xpress

Physical I/O