Cortex-A75 and Cortex-A55 DynamIQ processors

Powering applications from mobile to autonomous driving

Lionel Belnet | Sr. Product Manager | Arm
Agenda

• Market growth and trends
• DynamiQ technology
• Arm Cortex-A75 and Cortex-A55 processors
Arm: The industry’s architecture of choice

- 50 billion chips shipped in 1991
- 50 billion chips shipped in 2013
- 100 billion chips expected to ship in 2021

22 years between 1991 and 2013
4 years between 2013 and 2017
4 years between 2017 and 2021
50 billion chips shipped
Looking ahead from edge to cloud

Cortex beyond mobile

Safe and autonomous

Mixed reality

Hyper-efficient

Secure private compute
Arm architecture for total computing

Cortex-A
Highest performance
Designed for high-level operating systems

Cortex-R
Faster responsiveness
Designed for high performance, hard real-time applications

Cortex-M
Smallest/lowest power
Designed for discrete processing and microcontrollers

SecurCore
Tamper resistant
Designed for physical security
Innovating for the scalable future

Key Arm technologies

- NEON
- AMBA
- big.LITTLE
- CORELINK
- TRUSTZONE

Expanding Arm technology processor architecture for broad market

- Up to 8 CPUs “Octacore” smartphones
- Dual cluster
- Heterogeneous processing

Nearly “Unlimited” design spectrum

- Covers all existing use cases
- DynamiQ cluster
- Dynamic flexibility

2013 → 2017
DynamIQ technology
Imagine the possibilities
Arm DynamIQ
Rearranging the compute experience

**Designed from the ground up for AI**

**Large system performance uplift**

**More intelligent systems**
Accelerating AI adoption everywhere
DynamIQ boosting AI/ML performance with Arm Compute Library, latest CPUs and GPU

Mali GPU

Cortex-A CPUs

Accelerator

Dedicated processor instructions and optimized libraries for AI

Improved access to acceleration
Uncompromised performance at all tiers
DynamIQ increases big.LITTLE performance levels

High end
4b+4L
Laptop-ready compute performance

Mid
1b+7L
2x single-thread performance (vs. today’s octacore)

Entry level
4L
Elevating your user experience

Example configurations shown
Intelligent power savings

- **CPU**: Finer-grained speed control
- **Power States**: Faster on/sleep/off
- **CPU memory**: Autonomous power management
DynamIQ: New single cluster design for new cores

DynamIQ big.LITTLE systems

- Greater product differentiation and scalability
- Improved energy efficiency and performance
- SW compatibility with Energy Aware Scheduling (EAS)

Private L2 and shared L3 caches

- Local cache close to processors
- L3 cache shared between all cores

DynamIQ Shared Unit (DSU)

- Contains L3, Snoop Control Unit (SCU) and all cluster interfaces

Example: DynamIQ big.LITTLE configurations
Cortex-A75 and Cortex-A55 CPUs
DynamIQ-based CPUs for new possibilities

Cortex-A75 processor

>50%
more performance compared to current devices

Cortex-A55 processor

2.5x
higher power efficiency compared to current devices

Estimated device performance using SPECINT2006, final device results may vary.
Comparison using Cortex-A73 at 2.4GHz vs Cortex-A75 at 3GHz.

Comparison using Cortex-A53 in 28nm devices vs Cortex-A55 in 16nm devices.
DynamIQ-based CPUs for new possibilities

<table>
<thead>
<tr>
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<th>Cortex-A75</th>
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<th>Cortex-A55</th>
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<tr>
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<td><strong>Baseline to Cortex-A73</strong></td>
<td><strong>Baseline to Cortex-A53</strong></td>
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<td>Geekbench v4</td>
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*All comparisons at iso process and frequency*
L2 memory system

Common features

- Private L2 cache in each core
- Running at core speed
- Exclusive data cache
- Cache stashing into the L2
- Non-blocking 1024-entry TLB for hit-under-miss

Cortex-A75

- 256KB / 512KB

Cortex-A55

- 0KB / 64KB / 128KB / 256KB
System solutions
Premium Mobile System

Complete system IP portfolio from Arm

- Built for premium
- Scaled to mid-range and entry level

Incorporates the latest features

- Security with Arm TrustZone
- Sensor hub and acceleration

Related components:
- Cortex-A75
- Mali-G72
- Cortex-A55
- Mali-V61
- Sensor fusion hub Cortex-M7
- CoreLink CCI-550
- GIC-600
- Memory system, integrated TrustZone
- MMU-600
- DMC-500
- LPDDR4
- NIC-450
- Crypto Cell-712
- AD-5
- MMU-600
- Peripheral components
The best upgrade path for mid-range devices
Power, performance and area of octa-core CPU systems

<table>
<thead>
<tr>
<th></th>
<th>Cortex-A53 Octa</th>
<th>Cortex-A55 Octa</th>
<th>Cortex-A75/Cortex-A55 Octa</th>
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<tr>
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<td>Floating Point</td>
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<td>2.34</td>
<td>3.58</td>
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<tr>
<td>Memory Streaming</td>
<td>2.34</td>
<td>4.06</td>
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</table>

- **Area**: Computed using SPECINT2000 integer, SPECFP2000 floating point and JMCStream memory streaming benchmarks.
- **Performance**: 2-4x compared to Cortex-A53 LITTLE only.
- **Area**: Same or similar area compared to Cortex-A53 LITTLE only.

**Legend**
- Yellow: Area
- Dark Grey: Integer
- Light Grey: Floating Point
- Light Blue: Memory Streaming

**Note**: Coherent Interconnect for all configurations.
Safer autonomous systems

DynamIQ supports safety critical industrial and automotive systems

- Resilient systems
  - Allowing systems to operate safely under failure

- Adaptive compute
  - Uncompromised performance for autonomous systems

- Faster responsiveness
  - Quicker safety critical decision-making
Diverse range of automotive compute solutions

- **Vision ADAS**
  - Cortex-A55 + Cortex-R52
  - Heterogeneous multi-core
  - Computer vision
  - Control

- **Infotainment**
  - Cortex-A75 + Cortex-A55
  - Energy-aware scheduling
  - Rich OS
  - Security

- **Powertrain**
  - Cortex-R52
  - Real time
  - Homogeneous multi-core

- **Autonomous driving**
  - Cortex-A75 + Cortex-R52
  - High performance multi-cluster
  - Machine learning
  - Functional safety

- **Central body control**
  - Cortex-M7, Cortex-M0+
  - Low power
  - Efficient performance
  - Scalable

- **Other modules**
  - V2X
  - Chassis
  - Security
  - Radar
  - Sensor
  - Audio
Safety and reliability with DynamIQ

Compute performance for ADAS and IVI

- Higher performance for autonomous cars
- Faster responsiveness for safety critical tasks

Functional safety

- ASIL D systematic capability
- Advanced RAS architectural features

Industry’s broadest functional safety capable CPU IP portfolio
Power-Constrained ADAS Platform

- Isolated for highest reliability & integrity
- System monitoring, diagnostics & recovery
- Failsafe communication
Summary

DynamIQ technology is enabling more capable SoCs for key growth markets

• Brings new device solutions for all markets & tiers – from mobile to automotive, and beyond

Cortex-A75: Breakthrough performance – Cortex-A55: Efficiency redefined

• Elevating the user experience for the premium – doubling the performance levels for the mid-range and mass-market

New single cluster approach for better scalability and flexibility

• New DynamIQ Shared Unit, new memory hierarchy, new advanced power management features
Thank You!
Danke!
Merci!
谢谢!
ありがとうございます!
Gracias!
Kiitos!