Strato and Strato OS

Your new weapon for verification challenge

Justin Zhang
Senior Applications Engineering Manager

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Emulation Market Evolution

- Emulation moved to Virtualization with Veloce2
  - Data center friendliness
  - Enterprise level usage

- Veloce Strato accelerates
  - Moved to Application age
    - Emulation as a virtual resource
  - Cost Of Ownership reduction
  - Vertical market focus
Veloce Strato Announcement

Subject: SCOOP -- will the new MENT Veloce Crystal 3 chip crush Palladium?

From: [John Cooley of DeepChip.com]

My rudimentary understanding is:

- The new Crystal 3 uP is not Boolean based (like Palladium is), and it's not FPGA based (like Zebu is) -- but some sort of weird mystery hybrid of the two architectures?

- Claims that this mystery hybrid approach lets Strato have both "power efficiency" which Palladium lacks, but Zebu has; plus "visibility" which Zebu lacks, but Palladium has.

- Since Strato is not an FPGA chip, it's roadmap is not tied to the Xilinx technology roadmap.

Mentor Graphics Announces Veloce Strato Platform Scales Up to 15BG

WILSONVILLE, Ore., February 16, 2017 – Mentor Graphics® Corporation (NASDAQ: MENT) today announced the Veloce® Strato™ emulation platform. The Veloce Strato platform is Mentor’s third generation data-center friendly emulation platform, and the only emulation platform on the market with full scalability across both software and hardware. As part of the announcement, Mentor® is launching the Veloce Strato™ high-capacity emulator and Veloce Strato OS enterprise-level operating system.
Veloce Strato: Value Proposition

- **Best ROI**
- **Lowest COO**

**Capacity Scaling**
(2.5BG to 15BG)

**5x Productivity**
(3x Compile, 3x Bandwidth, 10x TTV)

**Data Center Friendly**
(Footprint, Air Cool, 1/3 Power/Gate, Uptime/Service)

**Easy Adoption, Migration and Use**
(Same Scripts, Apps, Use Model, Flows & Resource Efficient)
Veloce the Complete Verification Platform

- Fault
- Virtual Network
- Deterministic ICE
- DFT
- Enterprise Server
- Power
- Coverage/Assertions
- SW Debug
- Protocol Solutions (VirtualLAB, iSolve, Soft Models)
- Visualization

Veloce Strato OS SW

Core Compiler (Synth, Partition, PnR)
Use Modes (ICE, TBX, Virtual)
Debug (Live waveform, Replay)

Veloce Apps

Veloce StratoM
2.5B Gate

Maximus
1B Gate

Quattro
256M Gate

Veloce Strato
Up to 15B Gate
Veloce Strato Platform

■ Best Productivity
  — Up to 5x compile-runtime-debug productivity gain
    - Faster compile: up to 3x with 100% success rate
    - Faster time to visibility: up to 10x
    - Faster co-model bandwidth: up to 3x
  — SW and applications methodology and model reuse
  — Largest portfolio offering for Virtual and ICE
  — Lowest Cost Of Ownership

■ Largest Effective Capacity
  — Only platform that scales capacity to customer design needs
  — Only platform with roadmap up to 15 B Gates
Why Apps?

1. Structured set of features for specific needs
2. Easy to use interface
3. Customization
4. Platform independent
Veloce the Complete Verification Platform

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**Veloce Strato OS SW**
- Core Compiler (Synth, Partition, PnR)
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**Veloce Apps**

- Veloce StratoM 2.5B Gate
- Maximus 1B Gate
- Veloce StratoM 2.5B Gate

**Veloce2**
- Quattro 256M Gate
- Up to 15B Gate
Veloce Power App

- Low power verification at SoC level where power controls come from application SW
- Handle Large SoC (RTL/Gate) with Full Visibility
- Performance for Complete Verification (e.g. OS Boot) [100s of Millions of Cycles]
- Accurate Power Numbers based on real switching activity

<table>
<thead>
<tr>
<th>Design</th>
<th>Size</th>
<th># Cycles</th>
<th>File Flow</th>
<th>API Flow</th>
<th>X Factor</th>
</tr>
</thead>
<tbody>
<tr>
<td>PCI Subsystem</td>
<td>42MG</td>
<td>11M</td>
<td>40 hours</td>
<td>5 hours</td>
<td>8x</td>
</tr>
<tr>
<td>Processor</td>
<td>65MG</td>
<td>15 M</td>
<td>51 hours</td>
<td>6 hours</td>
<td>8.5X</td>
</tr>
<tr>
<td>Video Enc-Dec</td>
<td>35MG</td>
<td>72 M</td>
<td>90 hours</td>
<td>8.5 hours</td>
<td>10.5x</td>
</tr>
</tbody>
</table>

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Low Power Management (UPF)

Veloce Running Full SoC

Embedded SW Running on Processor

Processor

Power Control Block

Power control from SW

Multimedia (#3)

Memory (#2)

Storage (#5)

Ethernet (#4)

USB (#1)

SW Driven Power Management Validation

Design
- RTL & Gate
- UPF 1/2/3
- Liberty Support

Memory
- ON
- OFF
- Standby

Debug
- Static & Dynamic checks
- Coverage
- Visualizer Power Console
Power Analysis

Identification of Power peaks
Large peaks (~1us) -> e.g. Supply integrity
Narrow peaks (~1ns) -> e.g. IR-Drop

Verification of Power Domains Usage via UPF

Power Surges Identification
\(\frac{dI}{dt}\) voltage drop

Electro-migration
High power on very long periods

Hot Spots Identification
Optimization targets, Local IR-Drop,…

Power Trends
Compare activity plots across RTL drops

Signoff Power Plot
Close Correlation
Veloce Activity Plot
Current DFT Verification Scenario

- All the teams are competing for the same CPU resources
- Functional and Physical verification take priority for CPU access during tape-out
- DFT verification (Unit Delay and SDF) takes a long time, when time is limited
- Tapeout signoff happens with incomplete DFT verification
Veloce DFT App: Accelerate DFT Verification

- Accelerate unit delay patterns using Veloce
  - Achieve faster overall DFT verification
  - Ensure entire DFT verification flow is done before tape-out signoff

Simulate patterns with SDF back annotated using CPU farm
Veloce DFT App

- Verify DFT logic and BIST structure
- Increase pattern correctness, robustness, reliability (STIL and WGL)
- Pre-tapeout pattern validation, accelerate time to production
- Reduce ATE test time and costs

Design  | DFT Simulation | Veloce DFT | Improvements
---|---|---|---
Sensor  | 3.1 days | 90 sec | 3000x
WideIO  | 83.3 days | 2 hours | 1000x
Graphics | 2.7 days | 58 sec | 4000x

Improve Manufacturing Ramp-up and Time-to-Yield
Veloce Fault App

- Emulates design behavior in presence of structural faults
- Measures Fault Tolerance of the design
  - Inject different types of structural faults
    - Types: Stuck at 0/1, Transition, Bridging fault
    - Monitors effects of faults
- Automates comparison of values from a golden run (no Faults) vs a faulty run
  - Reports mismatches at runtime
- Important for safety critical industries (automotive, aerospace, military)
Veloce Coverage App

- Hard-to-reach corner cases requiring millions of clock cycles
- Coverage collection using real-world stimulus
- Boot OS and collect coverage while running software
- Coverage for safety compliance
Veloce Deterministic ICE App

- Unique offering for Veloce ICE emulation
- Delivers repeatable behavior for ICE debug
- LiveStream generates waveform for entire ICE run
- Apps: Power, Coverage, ...

Boost productivity for the traditional ICE use mode
Strengthen ICE offering and enable path from ICE to Virtual
Visualizer App

- Common platform for Veloce and Questa
- Short learning curve for transition from other debugger
- Biometric search, driver tracing, memory view, ....
Job Management for Veloce : ES App

[Diagram showing job management with different types of jobs: Large Jobs, ICE Jobs, Accln Jobs, and Priority Jobs. The Job Queue is represented with statuses: Busy, Free, and Reserve.]
Enterprise Server App

- Maximize Veloce utilization & sharing
- **Automated** job scheduling & prioritization
- Flexible Veloce sharing by multiple teams worldwide
- On-the-fly utilization reports
- Support LSF, SGE, NC or custom
Veloce VN App

- Unified pre/post-Si development and test platform
- Virtual Machine: ease of use, debug, analyzers, SW configurable
- Post-Si traffic fidelity and statistics in pre-Si verification
Configurable IP Reference Platform

Driving SW Development Costs Down
Access to Configurable IP Reference Platform

- A complete open source stack
  - Linux drivers to Android apps
  - Benchmarks on OS
  - Customized for vertical market segments

- Running on a configurable virtual platform
  - Pre-configured for fast hybrid emulation with Veloce
  - Fast OS boot>>>HW Accurate
  - Common peripherals for the target market segment

- Full instrumentation for hardware, software, power, and performance debug

Full system level validation in the context of real software

Example Android OS Boot and GPU Benchmarking

<table>
<thead>
<tr>
<th>Activity</th>
<th>PLAID Time</th>
<th>RTL Emulation Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>Android Linux Prompt</td>
<td>3 min</td>
<td>18 min</td>
</tr>
<tr>
<td>Android Services</td>
<td>8 min</td>
<td>10 hr</td>
</tr>
<tr>
<td>Android Apps</td>
<td>10 min</td>
<td>&gt;24 hr</td>
</tr>
</tbody>
</table>

PLAID Hybrid Platforms
50X Emulation