Practical ARM® CPU Digital Implementation on TSMC 10nm

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Outline

• ARM + Cadence Collaboration
• 10nm Design (Synthesis, Implementation, Signoff) Challenges
• 10nm Design Flow for High-end ARM CPU Implementation
• Cadence® Advanced Node 10nm RTL2Signoff Flow and Unique Solutions
• Foundry Qualification of Cadence Tools
• Summary
ARM and Cadence Collaboration

- Ongoing close collaboration on ARM CPUs, ARM Mali™ GPUs, system IP, embedded processors, ARM Artisan® libraries, and ARM POP™ IP
- Cadence and ARM engineering relationship at all ARM design locations worldwide
  - Engineering teams at Cambridge/Sheffield, Sophia, San Jose, Austin, Bangalore, and Hsinchu
- Cadence and ARM have collaborated throughout the entire development of multiple cores to drive technology leadership in the ecosystem for power, performance, and area (PPA) goals (2011-2015)
  - Trial implementations being run in parallel by both ARM and Cadence
  - Regular interaction with Cadence AEs and R&D
- ARM uses Cadence® tools and flow internally for high-performance processor and GPU development
  - ARM + Cadence collaborative work-around reference flow development
  - Testchips currently include ARM Cortex®-A72, A57, A53, A15, A12, A9, and A7, plus POP IP and Cortex-M embedded processors such as M7 and others
ARM and Cadence Projects History

ARM and Cadence are successfully engaged in several joint projects.
ARM and Cadence
Collaborating on 10nm

- A global collaborative program to develop advanced process eco-systems
- Ensure ARM next generation CPU IP is optimized for advanced process
- Ensure EDA eco-system and design flows are ready for lead partners
- Provide feedback on power, performance and area bottlenecks to ARM design teams
- Identify additional physical IP requirements for optimal PPA
- Educate partners and accelerate next generation process adoption

*Proven successful approach following on from 16nm collaboration*
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Design challenges at 10nm

- Full coloring flow required in P&R, extraction, DRC
- Use of M1/M2 to be H/V impacts cell architecture and routability
- Significant increase of critical rules for router and placement

Physical
- Resistance increase on wire and vias (Mx and Vx).
- Variability (wire width, spacing)
  - Different color tracks may have dramatic resistance difference.
  - Length-based coupling cap handling
- Expect the need for more accuracy in timing and variation

Electrical

- Resistance increase on wire and vias (Mx and Vx).
- Variability (wire width, spacing)
  - Different color tracks may have dramatic resistance difference.
  - Length-based coupling cap handling
- Expect the need for more accuracy in timing and variation
Accelerating 10nm Adoption

• Start early so that IP, tools and process can be optimized at the same time

• Ensure ARM IP, process and EDA tools are co-optimized to:
  – Provide best in class silicon implementations of ARM based systems
  – Pipe-clean the eco-system for ARM partner designs
  – Lower the barrier to entry for new process adoption
  – Reduce time to market through optimized products and support
ARM CPU 10nm Challenges

An evolution from 16nm FinFET

• Focus on efficiency
  – Optimize performance within established mobile device power budgets

• Power grid integrity is crucial
  – Meeting electromigration and IR drop targets whilst maintaining placement density

• Interconnect (wire) resistance continues to dominate
  – Use of optimized physical libraries more critical

• Maximize the benefits of process scaling
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Design Flow Considerations

- Understand critical differences between 16nm and 10nm design flows

- Primary goal is to tweak the flow recipe and understand tool/IP interaction
  - Impact of new CPU uArchitecture
  - Feedback on tool, library, and IP interactions
  - Optimizing floorplan, power distribution, and overall power, performance and area

- Traverse the entire flow from RTL to production quality sign-off
  - All issues uncovered and validated

- Iterate and improve as IP, process, and libraries mature
Synthesis Strategy

- Exploration to understand power and performance envelope
  - Selecting the right $V_t$ mix for design PPA targets

- Analyze library usage for potential bottlenecks
  - Dominant cell type on critical paths

- Based on Cadence recommended flow
  - Tuning of parameters for optimal PPA trade-offs

- Physical aware mapping
  - Ensure correlation and predictability through flow

- Synthesis targets single $V_t$ and channel length
  - Based on performance and power targets
The Genus Advantage

- Significant run time and overall QoR benefits
- Improved correlation through the flow
- Increased performance with minimal leakage impact
- Synthesis run time over 4x faster (~3 hours)
Floorplan

• New process and processor combination
  - Floorplan trials are critical
  - Macro placement changes with process

• Use of placement regions based on uArchitectural feedback

• Macro placement needs to follow finFET grid

• Must align double pattern layer M2 memory pins to ensure correct coloring
Power Grid

• Incorrect power grid construction will *significantly* impact routing density and performance

• No metal 2-standard cell power connection
  – Potential EM and dynamic IR implications

• Vertical power straps need to follow FinFET grid

• Horizontal straps must follow even poly pitch

• Traditional “striped” PG methodology used
Place & Route

• Place and route uses single $V_t$/Channel length library

• Timing and power is optimized against dominant corners
  – Balance of run time vs overall QoR

• Placement is DRC aware
  – Respects interaction between standard cells

• Control of wire dominated paths is crucial
  – Using placement bounds to constrain potential long paths
  – Layer promotion for long nets to less resistive metal layers

• Waveform propagation models and AOCV essential at 10nm
Sign-Off

• Full production quality sign-off approach
  – TSMC recommended timing margins
  – Signed-off for timing, power integrity & physical rules

• Cadence® Voltus™ solution used for all power integrity checks
  – Static/dynamic IR, electro-migration, in-rush current

• Signed-off and optimized across multiple PVT and extraction corners

• Leakage recovery performed using Tempus™ ECO functionality

• Power analysis – early and often to ensure PG structure is correct

• Stage based OCV critical to avoid over-fixing
Design Flow

- Implemented using Cadence® tools
- Full production quality DFT solution
  - Full scan compression
  - Memory BIST
  - At speed scan and memory BIST support
- Power domain per CPU core
- Full production margins for timing, power and physical sign-off
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Cadence Full-Flow Digital Solution vs. Previous Generation

Traditional Flow
- placer
- router
- Opt
- CTS
- timing
- power
- extract

Synthesis
- Unified Placement Engine
- Best-in-Class PPA Optimization
- Unified Timing/Power/Extract

Implementation
- Unified CTS, Global Router
- Up to 10X TAT/Capacity Gain
- Full-Flow Correlation
- Design Convergence
- Early Signoff Opt
- Reduced iterations

Signoff
- Early Signoff Opt
- Reduced iterations

Massively Parallel
Unified Engines
Core PPA Algorithms

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Innovus Technology

GigaPlace™ next-generation placement

- Electrical-driven
- Physical-driven
- Optimization-driven

Slack-driven, layer-aware, fully analytic

GigaOpt™ power-driven optimization

- All GigaOpt transforms made power-aware
- Minimizes leakage, internal and switching power

Advanced CCOpt™ and slack-driven routing

- Flex H-tree improves cross-corner variation
- Slack-driven routing reduces SI TNS
Innovus: 10nm color-driven implementation

- Unique correct-by-construction approach
- Prevents odd-cycle conflicts
- Massively parallel for increasing rule conflicts
10nm color-driven placement and routing

Color-driven GigaPlace™ technology

NanoRoute™ via odd-cycle prevention

Actively prevents pin-access that causes “odd-cycles”

Status of SADP-enabled Innovus System

<table>
<thead>
<tr>
<th>Function</th>
<th>Status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Color-aware placement</td>
<td>cell-flip, color-swap, and fill-cell demonstrated</td>
</tr>
<tr>
<td>Explicit via coloring</td>
<td>Color-conflict free routing demonstrated</td>
</tr>
<tr>
<td>Fill-wire generation</td>
<td>DRC-clean fill wires demonstrated</td>
</tr>
<tr>
<td>Ultra-regularized Mx-cuts</td>
<td>80-95% utilization demonstrated DRC clean</td>
</tr>
</tbody>
</table>
Color-driven GigaPlace technology

- Fixed color placement
- **Vertical** edge constraints
- Placement considering power buses and power bus via
- Global placement for routability improvement
- Boundary (endcap) cell insertion
Color-driven NanoRoute technology

- All 10nm rules.
- Enhance **pin access** to handle large same-mask cut spacing.
- Fat M2 pin handling: track alignment and rules.
- Fixed color methodology: users define color/mask in cell library
- M1 routing.
- One side spacing of NDR, mask-NDR
Production-proven Genus and Innovus speedup

Genus™ TAT speedup

- <= 16nm CPU > 2GHz 1.3M: 3.1X
- 28nm GPU 500MHz 4.9M: 4.8X
- <= 16nm Networking < 2GHz 1.0M: 5.5X
- <= 16nm 600MHz 2.9M: 3.6X
- 28nm GPU 400MHz 3.2M: 3.5X
- 28nm DSP 600MHz 2.0M: 4.1X

Innovus™ turnaround time (TAT) speedup

- 9.3M Cell 28nm: 9.7X
- 2.8M Cell 28nm: 7X
- 3.1M Cell 28nm: 6.9X
- 5.5M Cell 16nm: 6.1X
- 1.5M Cell 16nm: 5.2X
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10nm color-driven Cadence digital flow

**Innovus™ Implementation System**
- PreRoute Statistical RC Extraction
- Statistical OCV-driven Optimization
- Color-Aware Track Assignment

**Quantus™ QRC**
- 10nm extraction certification
- Colored aware resistance change
- Length based coupling cap handling.

**Tempus™, Voltus™, PVS Solutions**
- 10nm STA qualification, SOCV, SOCV-Driven
  MMMC Sign-Off ECO
- Color-aware EM/IR
- Color-aware Metal Fill, Fill ECO

_Cadence Digital and Custom/Analog Tools Achieve TSMC Certification for 16FF+ Process, Companies Collaborate on 10nm FinFET_

**10nm FinFET Process Collaboration Enables Immediate Early Customer Design Starts**
SAN JOSE, Calif., 26 Sep 2014

_Cadence Digital and Custom/Analog Tools Achieve TSMC Certification for 10nm FinFET Early Design Starts_
SAN JOSE, Calif., 26 Apr 2015

"We worked closely with Cadence to certify tools for customers to enjoy the benefits of higher performance and lower power consumption of TSMC’s 16nm FinFET Plus process,” said Suk Lee, TSMC senior director, Design Infrastructure Marketing Division. “The design tools and manufacturing process have been tested to ensure they work seamlessly together so that customers can achieve reduced iterations and improved predictability. Moreover, we are actively collaborating with Cadence on the 10nm FinFET process, and the joint flow is ready for early customer designs."
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• Cadence and ARM continue to collaborate on advanced process nodes

• Our proven successful collaboration model accelerates adoption and time to market for our partners

• 10nm has arrived, and the eco-system is ready for your next ARM-based chip
Come visit us in Cadence Booth